SUBSTITUTE SPECIFICATION: CLEAN COPY
U.S. PATENT APPLICATION NO. 10/662,122

TITLE OF THE INVENTION:

Method for Detecting an Octet Slip

CROSS REFERENCE TO RELATED APPLICATIONS:

[0001] This application claims priority of United States Provisional Patent Application Serial No. 60/464,113, entitled "Method for Detecting an Octet Slip," filed on April 21, 2003, the contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION:

Field of the Invention:

[0002] The invention relates to pulse code modulation in telecommunication systems. In particular the present invention concerns a method for detecting a frame slip.

Description of the Related Art:

[0003] In general, core networks of modern telecommunication systems are digital. However, the last mile connection is typically an analog twisted-pair cab e. In a pair cable the received and sent signal is transmitted in the cable simultaneously. Thus cable resources are saved compared to a four lead cab e. As the fixed line terminals are typically analog terminals, a signal conversion

from analog to digital and vice versa is required.

[0004] PCM (Pulse Code Modulation) is a digital scheme for transmitting analog data. The PCM-signals are binary, that is, there are only two possible states, represented by logic 1 (high) and logic 0 (low). This is true no matter how complex the analog waveform happens to be. Using PCM, it is possible to digitize all forms of analog data, including full-motion video, voices, music, telemetry, and virtual reality.

[0005] To obtain PCM from an analog waveform at the source (transmitter end) of a communications circuit, the analog signal amplitude is sampled (e.g., measured) at regular time intervals. The sampling rate, or number of samples per second, is several times the maximum frequency of the analog waveform in cycles per second or hertz. The instantaneous amplitude of the analog signal at each sampling is rounded off to the nearest of several specific, predetermined levels. This process is called quantization. The number of levels is always a power of 2, for example, 8, 16, 32, or 64. These numbers can be represented by three, four, five, or six binary digits (bits) respectively. The output of a pulse code modulator is thus a series of digital samples that are binary numbers, each having some power of 2 possible different values.

[0006] At the destination (receiver end) of the communications circuit, a pulse code demodulator converts the digital samples back into pulses having the same quantum levels as those in the modulator. These pulses are further processed to restore the original analog waveform. If the sampling rates of the modulator and demodulator are not exactly the same, eventually the demodulator is going to

receive some digital sample earlier or later than it is expecting. This is called frame slip. As a result of a frame slip one digital sample in the series of samples is lost (negative slip) or one sample is repeated twice in (positive slip). The effect on the analog waveform is as if the frequency of the analog waveform changed momentarily by relatively small value.

[0007] In a telecommunication network there are several pieces of equipment located between the modulator and demodulator in the transmission path of the pulse code modulated signal. Each of these pieces of equipment may have different clock rate. In order to minimize the effect on the analog waveform unsynchronized digital signal processing equipment occasionally has to duplicate or delete one digital sample. As a result pulse code modulated signals in telecommunication networks have frame slips.

[0008] ETSI TS 101 504 V8.0.1 (2000-08) standard, which is included here by reference, describes an inband signalling protocol between transcoder and rate adapter units for speech traffic channels in tandem free operation of speech codecs. In this protocol communications are handled with inband signalling messages. Inband signalling messages are transmitted by replacing the least significant bit of some of the digital samples by a bit of inband signalling message. In the standard, digital samples are called octets because they consists of 8 bits and the interval in which the least significant bit of octet is replaced is defined to be 16 samples. Generally similar inband signalling can be carried in the least significant bit of every Nth digital sample and digital sample can be some other number of bits than 8. Furthermore the standard defines inband

signalling messages to be constructed of 20 and 10 bit long blocks. Generally N bit long mocks can be considered.

[0009] The standard discloses several error detecting and correcting situations based on the limited number of allowed 20 or 10 bit blocks among all possibilities of 20 or 10 bit blocks. The standard suggests assuming hypothetical octet slip for finding error-free or single-error message. An octet slip is a situation in which sequence of octets has slipped one octet forward or backward. As a result a block of inband signalling bits taken from least significant bit of every 16^{th} octet contains only the first part of the intended 20 or 10 bits. Bits that arrive after the octet slip have shifted into an adjacent block can be found in the least significant bit of every preceding or succeeding 16^{th} octet. If an error-free or a single-error inband signalling message can be found after considering a hypothetical octet slip (±l octet), then it may be regarded as error-free or single-error and the new phase position will be regarded as valid provided that no valid or present inband signalling message can be found at the old phase position. However, even though the standard suggests assuming the octet slip, it does not provide any means for detecting an octet slip within inband signalling block.

[0010] One solution for detecting an octet slip is to take first k bit of the inband signalling message block from found PCM sample grid and 20-k or 10-k last bits from the ±1 position and join the k bit field with 20-k or 10-k bit field to form the octet slipped block and calculate the number of error bits. Because the time of the octet slip is not known beforehand in the worst

case this has to be repeated for all values of k = 1 ... 20 or 10 until right value of k is found. Figure 1 illustrates an example situation where k = 4. Bits a are the least significant bits of previously found 16 octet grid. Bits b are the least significant bits of preceding or succeeding 16 octet grid. Normally the 10 bit block of inband signalling message should consist of the a bits. However because of an octet slip somewhere between bits 4 and 5 the last bits of block appear in b bits instead. A device that is supposed to interpret inband signalling messages does not know in advance at which point the octet slip has occurred. Therefore it has to try to match different combinations of a and b bits with acceptable bit patterns before it finds out , for example, that a combination of the first 4 a bits and 6 last b bits produces expected result. For N bit block there are N different possibilities where octet slip may have occurred. Therefore there are N different combinations of a and b bits. The investigation of whether a combination is right or not takes time proportional to N.

[0011] The drawback of the above-described solution is the $0(N^2)$ complexity. $0(N^2)$ complexity means that time required to compute the algorithm is related to the square of the input size. Thus there is obvious need for an efficient method for detecting an octet slip in an inband signalling block.

[0012] Accordingly, it would be desirable to have a more efficient method for detecting an octet slip in pulse code modulation in telecommunication systems.

SUMMARY OF THE INVENTION:

[0013] The invention discloses improved methods for detecting an assumed

octet slip in an inband signalling block in pulse code modulation. Octet slip **is** assumed for detecting possible phase shift. In one aspect of the invention, octet slip is detected by processing two different bit blocks that are collected from the least significant bit of every 16th octet. The block that would usually, under errorless circumstances in case of no octet slip, correspond to the sample block that is expected to be found, is referred as a signalling block. The block where expected bits have transferred into after the octet slip is referred as an adjacent block.

[0014] The adjacent block includes bits that are collected from the least significant bit of every octet before or after the octet which carries the bit of the signalling block. When negative octet slip is searched the adjacent block contains the bits from the predecessor octets of the octets occupied by signalling block. When positive octet slip is searched the adjacent block contains the bits from the successor octets. Accordingly, one embodiment of a method of the invention includes searching error bits in the signalling block and counting error bits of the adjacent block.

[0015] The octet slip is observed by analyzing error count and searched error bits. Searching the error bit is done by comparing the signalling block to a sample block. The error count for adjacent block is started from the first error bit k1 of signalling block. If error count of adjacent block is zero or one, the octet slip may have happened before error bit kl. If error count is more than one the octet slip may have happened from or after the error bit k 1. If the error count is more than one, a second error bit k2 of signalling block is searched starting from

bit k1+1 When second error bit k2 is found, the bits of the adjacent block starting from the second error bit k2 are verified. If the bits starting from k2 are correct, the octet slip is between error bits k 1 and k2 and the error count is one. Otherwise the error count is more than one and octet slip cannot be detected.

[0016] One benefit of the present invention is the efficiency compared to 6(N^2) complexity of the prior solution. Furthermore a benefit of the invention is that it can be easily implemented as present digital signal processors include capabilities for comparing and searching the first error bit.

BRIEF DESCRIPTION OF THE DRAWINGS:

[0017] The accompanying drawings, which are included to provide a further understanding of the invention and constitute a part of this specification, illustrate example embodiments of the invention and together with the description help to explain the principles of the invention. In the drawings:

[0018] Fig. 1 is a prior art illustration of one step in an obvious solution for detecting an octet slip;

[0019] Fig. 2A is a flow chart of an example embodiment of the present invention;

[0020] Fig. 2B is a flow chart of an example embodiment of the present invention; and

[0021] Fig. 3 is a block diagram illustrating one embodiment of a system according to the present invention.

[0022] Fig. 4 is a block diagram illustrating one embodiment of a system

according to the present invention.

[0023] Fig. 5 is a block diagram illustrating one embodiment of a system according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT(S):

[0024] Reference will now be made in detail to the embodiments of the present invention, examples of which are illustrated in the accompanying drawings.

[0025] In figures 2A and 213 a flow chart of a method according to one aspect of the present invention is represented. A method for detecting an octet slip in an inband signalling block in pulse code modulation includes searching and counting error bits from the signalling block and adjacent block. Figure 2A represents an optional part of the present invention that is not required in the preferred embodiment. The method starts by choosing the searching direction in step 210. If searching is decided to start from the last bit in step 211, the signalling block is checked first to see if it is completely error free in step 212. After checking, the blocks are set in step 213. If the searching is started from the last bit to the first bit the error bits are counted from the signalling block. If the searching is started from the first bit the error bits are counted from the adjacent block. In one preferred embodiment the search is started always from the first bit.

[0026] The octet slip is observed by analyzing error count and searched error bits. Searching of the error bits is done by comparing the signalling block to a sample block, step 20. If no error bits are found in said searching, the block was

correct and no further actions are needed, steps 21 and 22. Searching can be made for example by performing XOR-operation to signalling block with sample block so that in a result the correct bits are zeros and the erroneous bits are set to ones. The set error bits can be easily detected by hardware. Complexity of searching the first error bit is proportional to the amount of the bits before kl.

[0027] If an error bit is found, the following step is to count the amount of errors in the adjacent block starting from the bit after k1 in step 23. Again error bits can be set to one by a XOR-operation of adjacent block with sample block. The error count is simply the sum of 1 bits. Because upper limit for error is known to be 1 counting of all bits is not necessary. Counting can be stopped when an error count of 1 has been reached. Complexity of counting is proportional to N-k1, in which N is the amount of the bits in the signalling block. If the error count is zero or one, step 24, the octet slip may have happened before error bit kl, step 25. If the error count is more than one the octet slip may have happened from or after the error bit k1 and second error bit k2 is searched in step 26. The complexity of searching the second bit is proportional to k2-kl. The error bit k2 is searched starting from bit kl+1. When second error bit k2 is found in step 26 the bits of the adjacent block starting from the second error bit k2+1 are verified in step 27. The complexity of verifying is proportional to N-k2. If the bits of the adjacent block starting from k2 are correct in step 28, the octet slip is assumed between error bits kl and k2 and the error count is one in step 30. Otherwise the error count is more than one and octet slip can not be assumed in step 29. As the method does not have internal loops the overall time needed for computations in a worst case

is proportional to kl+(N-kl)+(k2kl)+(N-k2). Thus the method is considered to be very efficient.

[0028] In figure 3 an embodiment of the present invention is represented. Advantageously the invention is implemented with in the IPE (In Path Equipment) 30. IPE is arranged between the sender 35 and receiver 36. Types of the IPE are discussed in annex B.1 of the ETSI TS 101 504 V8.0.1 (2000-08) standard. Typical IPE is a switch, a link or a DTMF (Dual Tone Multi Frequency) generator. The octet slip assuming can be done with a separate module or an integrated module. In figure 3 the slip detector module 31 is separate. The slip detector module 31 is utilized when regular error detection of IPE 30 fails. This means a phase shift in a block so that there seems to be several bit errors even if in reality the only error is a phase shift of one PCM sample. Therefore a hypothetical octet slip is assumed.

[0029] A system for detecting an assumed octet slip in one embodiment includes the sender terminal 35, the receiver terminal 36 and the in path equipment 30. The octet slip is detected by a slip detector 31. In the preferred embodiment the slip detector is arranged into IPE 30. The slip detector 31 comprises three components that are a searcher 32, a counter 33 and a detector 34. The searcher 32 first searches first error bit k1 starting from the first bit of the signalling block. The searcher 32 searches bit error by comparing the signalling block to a sample block. The counter 33 is arranged to count the number of bit errors starting from said kl bit in the adjacent block. The detector 34 is arranged to detect the octet

slip by analyzing error bits in the adjacent block. The detector 34 detects the octet slip starting from or after the bit k1 if the number of the bit errors in the adjacent block is more than one. If the error count starting from the k1 is zero or one the octet slip is detected before the bit k1. If error count is more than one, the searcher 32 searches second error bit k2 starting from the bit after the first error bit kl. If the second error bit is found, the detector 34 verifies if the bits of the adjacent block starting from the second error bit k2 are correct. If the bits are correct, the octet slip is detected between error bits kl and k2. If the error count is more than one, the detector 34 cannot observe the octet slip. The searcher 32, counter 33 and detector 34 can be implemented in software. The system may be arranged to work similarly as the method of figure 2. Thus the system is capable of choosing the searching direction if desired. The system presented in figure 3 is an example of a preferred embodiment which searches always from the first bit.

[0030] In figure 4, an embodiment of the present invention is represented. The slip detector 31, as described above, may be arranged in the in path equipment 30.

[0031] In figure 5, an embodiment of the present invention is represented. The slip detector 31, as described above, may be arranged in the receiver terminal 36.

[0032] It should be noted that the method and the system applying the method described above works to both directions. This means that the first bit from where the searching is initiated may be the most significant or the least

significant bit. If searching is initiated from the last bit, the search is initiated from the adjacent block and the errors are counted from the signaling block. In this case it is best to check if the signaling block is error free. The algorithm works correctly in both cases. The method may be applied also in the terminal devices described by the above-mentioned ETSI standard chapter 8.4.2.

[0033] It is apparent to a person skilled in the art that with the advancement of technology, the basic idea of the invention may be implemented in various ways. The invention and its embodiments are thus not limited to the examples described above but instead is limited only by the scope of the claims.

[0034] One having ordinary skill in the art will readily understand that the invention as discussed above may be practiced with steps in a different order, and/or with hardware elements in configurations which are different than those which are disclosed. Therefore, although the invention has been described based upon these preferred embodiments, it would be apparent to those of skill in the art that certain modifications, variations, and alternative constructions could be made, while remaining within the spirit and scope of the invention.